REMARKS

Claims 1-4, 6-19, 21-24 and 26-30 stand rejected under 35 U.S.C. § 103 as being anticipated by U.S. Patent Number 5,859,999 by Morris (hereinafter " Morris") in view of U.S. Patent Number 4,484,271 by Miu (hereinafter " Miu").

Applicant thanks the Examiner for renumbering the claims as stated in CFR §1.126. Applicant makes reference to claims 4-10 as if they wee renumbered. Claims 11-28 maintained proper antecedent basis at the time of filing. Hence, renumbering them to 10-27 shall still maintain proper antecedent basis.

Reconsideration of this application is respectfully requested.

35 U.S.C. § 103 Rejections

In regards to claim 1, the Examiner states that "means and method of branching to a first location within programming code based upon the first logic value (e.g., see col. 1, line 12 – col. 2, line 11)" is met by Morris. Office Action, page 3. Applicant respectfully disagrees that Morris discloses branching to a first predefined location within programming code based upon the first logic value. Claim 1 states:

> 1. A method for restoring a memory value comprising:
> identifying a first logic value stored in a first register;
> branching to a first predefined location within programming code based upon the first logic value;
> utilizing the first register as a scratch register during execution of the
> programming code;
> restoring the first logic value back to the first register after execution
> of the programming code has finished.
>
> (Emphasis Added)

Applicant respectfully submits that Morris fails to disclose, "branching to a first predefined location with programming code based upon the first logic value." In contrast, Morris merely discloses that conditional executions of instructions may be implemented via the branch or jump instruction, which is well known in the art. "In traditional computer systems condition execution is implemented via the branch or jump instruction well known in the art." Morris, col. 1, lines 19-27. Morris is not specifically disclosing a branching to a first predefined location within programming code based upon the first logic value. Morris merely mentions that the concept of branching exists in general. Morris explicitly fails to disclose branching to a predefined location within programming code. In fact, Morris is completely silent on a predefined location.

In another distinction from claim 1, Morris also fails to disclose that a branch to a predefined location within programming code is based upon a first logic value that was previously identified in a first register. In contrast, Morris merely mentions that under predicate execution, a predicate may have a value of true or false, such that a zero may represent false and a one may represent true. "Predicated execution is implemented by associating a "predicate" with an instruction where the predicate controls whether or not that instruction is executed. If the predicate evaluates to "true", the instruction is executed; if the predicate evaluates to "false", the instruction is not executed. The definition of "true" and "false" may vary with each embodiment. The function by which the predicate is determined to be true or false may also vary with each embodiment. For example, some embodiments may define the predicate to be a single bit where a value of one is true and a value of zero is false..." Morris, col. 1, lines 30-39. Morris fails to

disclose that an actual logic value was considered when branching to a location within programming code. Therefore, Morris fails to disclose, "branching to a first predefined location within programming code based upon the first logic value."

Applicant also submits that Miu also fails to disclose, "branching to a first predefined location within programming code based upon the first logic value." In fact, Miu is completely silent on branching to predefined locations with programming code. In contrast, Miu discloses "a hardware interrupt apparatus for assigning the micro-programmed control system to the highest priority hardware interrupt requesting service. Once the interrupt is completed, logic within each microinstruction indicates that the address of the next microinstruction should be taken from a hardware interrupt return address." Abstract. This is not the same as branching to a first predefined location within programming code based upon the first logic value. Therefore, Miu also fails to disclose this element of claim 1.

Furthermore, even if Morris and Miu were combined, such a combination would lack "branching to a first predefined location within programming code based upon the first logic value." By way of contrast, the combination of Morris and Miu would disclose a predicated execution of microcode dealing with software interrupt requests handled by CPU firmware.

Therefore, in view of the above distinction, neither Morris nor Miu, individually or in combination, disclose each and every limitation of claim 1. As such, claim 1 is not rendered obvious by Morris in view of Miu under 35 U.S.C. § 103(a).

Applicant respectfully submits that Morris does not suggest a combination with Miu, and Miu does not suggest a combination with Morris because Morris specifically

teaches away from such a combination. It would be impermissible hindsight to combine Morris with Miu based on applicants' own disclosure.

Claims 2-9 depend upon and include the limitations of claim 1. Therefore, the combination of Morris and Miu also fails to render claims 2-9 obvious under 35 U.S.C. §103(a).

Likewise, independent claims 17 and 21 include the limitation "branching to a first predefined location within programming code based upon the first logic value." As discussed above, the combination of Morris and Miu do not disclose, "branching to a first predefined location within programming code based upon the first logic value." As such, claims 17 and 21 are not made obvious by the combination of Morris and Miu under 35 U.S.C. § 103(a).

Claims 18-20 and 22-27 all depend upon and include the limitations of independent claims 17 and 21. Therefore claims 18-20 and 22-27 are also not made obvious by the combination of Morris and Miu under 35 U.S.C. §103(a).

In regards to independent claim 10, applicant respectfully asserts that the combination of Morris and Miu fail to render claim 10 obvious. The Examiner states that, "Miu however taught a processor abstraction layer including interrupt handler that saves architectural state code including [a] plural[ity] [of] predefined sections." Office action, page 5, item 16. Amended claim 10 states:

10. A digital processing system comprising:
an execution unit;
a general purpose register file coupled to the execution unit containing a plurality of general-purpose registers;
a memory coupled to the execution unit for storing a processor abstraction layer, the processor abstraction layer further including a plurality of interrupt handlers, each of the interrupt handlers further including saving architecture state code, the saving architecture state code further including a plurality of predefined sections, wherein each the predefined section corresponds to a logic value of a register whereby the logic value can be restored in response to the predefined sections.

(Emphasis Added)

Applicant respectfully submits that Miu does not disclose a processor abstraction layer further including a plurality of interrupt handlers, each of the interrupt handlers further including saving architecture state code, the saving architecture state code further including a plurality of predefined sections. First, Miu does not disclose a processor abstraction layer. In contrast, Miu merely discloses a CPU firmware. Miu, col. 30, lines 39-44. A CPU firmware is not the same as a processor abstraction layer.

Secondly, the CPU firmware of Miu also fails to include interrupt handlers that save architecture state code which includes a plurality of predefined state codes. In contrast, Miu merely discloses that, "the CPU firmware saves the current software state..." Col. 30, lines 53-54. CPU firmware that saves the current software state is not the same as interrupt handlers that save architecture state code. Lastly, Miu is completely silent on the architecture state code further including a plurality of predefined codes. In contrast, Miu merely mentions that CPU firmware saves the current software state, without any mention of including

a plurality of predefined state codes. Hence, Miu fails to disclose this element of claim 10.

Applicant also submits that Morris fails to disclose a processor abstraction layer further including a plurality of interrupt handlers, each of the interrupt handlers further including saving architecture state code, the saving architecture state code further including a plurality of predefined sections. In fact, the Examiner explicitly states, "Morris did not expressly detail an interrupt handler." Office action, page 5, item 16.

Furthermore, even if Morris and Miu were combined, such a combination would lack "a processor abstraction layer further including a plurality of interrupt handlers, each of the interrupt handlers further including saving architecture state code, the saving architecture state code further including a plurality of predefined sections." By way of contrast, the combination of Morris and Miu would disclose a CPU firmware micro-program that handles I/O interrupt processing.

Therefore, in view of the above distinction, neither Morris nor Miu, individually or in combination, disclose each and every limitation of claim 10. As such, claim 10 is not rendered obvious by Morris in view of Miu under 35 U.S.C. § 103(a).

Applicant respectfully submits that Morris does not suggest a combination with Miu, and Miu does not suggest a combination with Morris because Morris specifically teaches away from such a combination. It would be impermissible hindsight to combine Morris with Miu based on applicants' own disclosure.

Claims 11-16 depend upon and include the limitations of claim 10. Therefore, the combination of Morris and Miu also fails to render claims 11-16 obvious under 35 U.S.C. §103(a).

Conclusion

It is respectfully submitted that in view of the amendments and remarks set forth herein, the rejections and objections have been overcome. Applicants reserve all rights with respect to the application of the doctrine equivalents. If there are any additional charges, please charge them to our Deposit Account No. 02-2666. Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,
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